Amendments to the Specification

Please amend the title of the invention to read:

A1

CONDITION INDICATOR FOR USE BY A CONDITIONAL BRANCH INSTRUCTION

Please replace the paragraph beginning at page 12, line 7 with the following amended paragraph:

A2

During the 0Y stage, the IP of the preferred embodiment includes an Instruction Address Generate section 150 that provides logic that generates an absolute instruction address by adding a relative address to the address of a designated base register within the IP. A Jump Predict subsection 151, and an Instruction Address Generation subsection 152, provide absolute addresses to the Instruction Cache Tag Logic 153. The Instruction Cache Tag Logic 153 transfers the address to the Instruction Read Address Control logic 154, which resides in the Instruction Decode section 155, via interface 156. The Instruction Read Address Control logic 154 provides the address to the IP Instruction First-Level Cache (I-FLC) 38 [[30]] on address path 161 [[156]] to retrieve instructions, during the 1Y stage. The instructions are transferred to the Instruction Queue 159 over lines 157 where they are staged and begin decode during the 2Y stage.

Please replace the paragraph beginning at page 12, line 18 with the following amended paragraph:

A3

If the Instruction Cache Tag Logic 153 indicates that a cache miss occurred, the IP suspends execution. Lines 158 [[158a]] communicate the miss to the IP Memory Interface 160, which initiates a memory request to the SLC 42 [[34]] via Interface 40 [[32]]. When

R3 the instruction is returned via Interface 40 [[32]], it is provided on data path 33 [[32a]] to Instruction Queue 159 and to the I-FLC 38 [[30]] to be cached.